REMARKS

A final Office Action was mailed on July 30, 2004. Claims 1 – 14 and 47 are pending in the present application. With this Response, Applicants amend the specification, and amend claims 1, 2, 5, 8, 11 and 47. No new matter is introduced.

REJECTION UNDER 35 U.S.C. § 251

Claims 1 – 14 and 47 are rejected under 35 U.S.C. § 251 as being based on a Reissue Declaration that is defective for failing to address each of the errors corrected by the Reissue application and subsequent amendments (including, for example, amendments made in the present Amendment and the Amendment of August 26, 2003. Ina accordance with 37 C.F.R. § 1.175(b)(1), Applicants enclose a Supplemental Declaration For Reissue Patent Application To Correct Errors Statement, signed by Applicants, declaring that each and every error corrected in the present Reissue application not covered by the Reissue Declaration of January 26, 2001 arose without any deceptive intention on the part of Applicants. Accordingly, Applicants respectfully request that this rejection under 35 U.S.C. § 251 be withdrawn.

OBJECTION TO SPECIFICATION, CLAIMS

The specification is objected to at column 14, line 1 in regard to informalities. Claims 1, 2, 5, 8, 11 and 47 are also objected to in regard to informalities. Applicants thank the Examiner for suggesting amendments to the specification and these claims in order to overcome this rejection, and amend the specification and claims 1, 2, 5, 8, 11 and

47 in accordance with these suggestions. Applicants therefore respectfully request that the objection to the specification and to claims 1, 2, 5, 8, 11 and 47 be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 102

Claim 47 is rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,317,602 to Onoda et al. Claim 47 is also rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,535,252 to Kobayashi. Applicants respectfully traverse these rejections.

In independent claim 47, Applicants disclose:

> **47.** A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:
>
> an identifying circuit for identifying a demodulated signal at a predetermined identification level, said demodulated signal being obtained by demodulating a multilevel orthogonal modulated signal;
>
> a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit; and
>
> a clock phase detecting section for detecting a phase component of said signal identification clock, based on clock-phase-detecting composite input information including any one of (i) a combination of demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal and (ii) a combination of clock phase difference information to be supplied to said identifying circuit and signal error differential information obtained by said identifying circuit, and then supplying said phase component to said clock regenerating circuit,
>
> said clock phase detecting section including
>
> a difference detecting unit, responsive to the receipt of said composite input information, for detecting any one of (I) difference information between the demodulated signal and the equalized demodulated signal and (II) a combination of the clock phase difference information and the signal error differential information, and

a clock phase calculating unit for calculating said phase component of said signal identification clock based on the output from said difference detecting unit.

Significantly, independent claim 47 recites as a necessary component a clock phase detecting section for detecting a phase component of said signal identification clock, based on clock-phase-detecting composite input information including any one of (i) a combination of demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal and (ii) a combination of clock phase difference information to be supplied to said identifying circuit and signal error differential information obtained by said identifying circuit.

Onoda discloses a QPSK base-band delayed detector (see, e.g., FIG. 5 of Onoda). The detector of Onoda includes A/D converters 57, 58 for identifying and converting analog signals into digital signals and bit timing recovery (BTR) circuit 1 including phase comparison result detection unit 2 for detecting a phase component of the digital signals generated by converter 57, 58, and a digital PLL 3 for outputting a clock signal of appropriate phase. Unlike Applicants' claimed invention, however, Onoda fails to disclose that detection unit 2 detects either of a) difference information between the demodulated signal and the equalized demodulated signal, or b) a combination of clock phase difference information and signal error differential information.

Onoda nowhere discloses means to produce an equalized signal (for example, by means of an equalizing circuit), and therefore fails to disclose a detection unit that detects Applicants' claimed difference information between the demodulated signal and the equalized demodulated signal. In addition, Onoda fails to disclose a detection unit that detects Applicants' claimed combination of clock phase difference information and signal error differential information.

With reference to FIG. 5 of Onoda, Onoda discloses that I-channel data I' (a) moves from operation circuit 59 to flip flop (FF) 21, and that Q-channel data Q' moves from operation circuit 59 to FF 22. FF 21 samples a most significant bit (MSB) of the I-channel data I' (a) in synchrony with a data sampling clock signal (d) obtained from divider 34 (see, e.g., column 5, lines 54 – 61 of Onoda). As this MSB is not an error bit, the I-channel data I' (a) fails to correspond to signal error information, as is required by the present invention.

In addition, and again with reference to FIG. 5 of Onoda, the output of the divider 34 is data detecting a clock signal supplied to discriminators 60, 61 and parallel to serial converter (P/S) 62, and is not data detecting a clock signal supplied to analog to digital converters (A/Ds) 57, 58. As a result, while the detected clock signal may have clock phase information, it cannot have clock phase difference information, as is required by the present invention.

Kobayashi discloses a DQPSK clock synchronization circuit (see, e.g., FIG. 2 of Kobayashi). The circuit of Kobayashi includes A/D converters 41, 42 for detecting and converting analog signals into digital signals, phase detector error circuit 47 for detecting a phase error in the digital signals, and clock reproducer 48 for generating a clock signal m for A/D converters 41, 42. As in the case of Onoda, and in sharp contrast to Applicants' claimed invention, however, Kobayashi fails to disclose that detector circuit 47 detects either of a) difference information between the demodulated signal and the equalized demodulated signal, or b) a combination of clock phase difference information and signal error differential information.

Kobayashi nowhere discloses means to produce an equalized signal (for example, using an equalizing circuit), and therefore fails to disclose a detection unit that detects Applicants' claimed difference information between the demodulated signal and the equalized demodulated signal. In addition, Kobayashi fails to disclose a detection unit that detects Applicants' claimed combination of clock phase difference information and signal error differential information.

With reference to FIG. 2 of Kobayashi, Kobayashi discloses that a judgment timing clock signal l is supplied from the clock reproducer 48 to a judger 44 and the phase error detector 47. However, this judgment timing clock signal is not supplied to A/Ds 41, 42. The phase error detector 47 extracts judgment timing (a BTR pattern) from its outputs by means of a filter output I from band pass filter 46, and detects a phase error j with respect to a current judgment timing clock signal l (see, e.g., column 6, lines 57 – 61 of Kobayashi). As a result, the phase error detector 47 fails to detect clock phase difference information, as is required by the present invention.

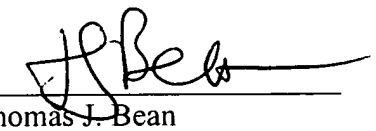
Accordingly, Applicants respectfully submit that claim 47 is not anticipated by either of Onoda and Kobayashi, and is therefore allowable.

CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that 1 – 14 and 47, which include independent claims 1, 2, 8 and 47, and the claims that depend therefrom, stand in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner should consider this

application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Respectfully submitted,



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